ABSTRACT

[0041] An apparatus for reducing CPU latency by reducing CPU bus read/write cycles, the apparatus includes a hardware register capable of testing data for one or more validity bits. A CPU is in communication with the hardware register during a first bus cycle and the CPU directs the hardware register to drive the data substantially simultaneously to the CPU and a second register. The data validity signal is performed in close proximity to the data transfer to the CPU and the second hardware device and the validity signal is forwarded to the second register without a subsequent bus cycle instruction to the second register from the CPU.